Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-7. (Canceled)

8. (Currently Amended) A structure formed in a substrate of monolithic semiconductor material, the structure comprising:

~~At~~ at least one trench formed in the substrate, the at least one trench having an open top and an open bottom;

a cavity having walls and a closed bottom formed below each at least one trench and having an open top in communication with the open bottom of the at least one trench, and a coating on the walls and closed bottom of the cavity with material inhibiting epitaxial growth; and

an epitaxial layer of semiconductor material integral with ~~grown horizontally and vertically on~~ the substrate to cover the open top of the at least one trench and formed in the at least one trench to fill the at least one trench and to encase the cavity in the substrate.

9. (Original) The structure of claim 8, comprising a plurality of trench and cavity pairs formed in the substrate.

10. (Original) The structure of claim 9, wherein each trench and cavity pair are formed at different levels within the substrate.

11. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have different cross-sectional configurations.

12. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have different cross-sectional sizes.

13. (Original) The structure of claim 9, wherein each trench and cavity pair are formed to have a different cross-sectional size and to be formed at different levels in the substrate.

14-18. (Canceled)

19. (Currently Amended) A structure formed in a substrate of monolithic semiconductor material, the structure comprising:

a cavity formed in and surrounded by the monolithic semiconductor material, the monolithic semiconductor material comprising a membrane ~~formed of an epitaxial growth of~~ integral with the monolithic semiconductor material ~~the monolithic semiconductor material that covers~~ to cover the cavity in the substrate, the membrane having a thickness in the range of between 1 and 3 μm.

20. (Canceled)

21. (Previously Presented) The structure of claim 19, further comprising at least one trench etched into the membrane and of a depth to be in communication with the cavity.

22-27. (Canceled)

28. (Currently Amended) A wafer of monolithic monocrystalline semiconductor material, comprising a plurality of buried cavities, each cavity completely surrounded by said monolithic monocrystalline material, including a membrane formed ~~of an epitaxial growth of~~ integral with the semiconductor material, and each cavity having walls and a closed bottom covered with a single coating formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned adjacent to each other and separated from each other by dividers.

29. (Previously Presented) The wafer of claim 28, wherein the material inhibiting epitaxial growth comprises oxide.

30. (Previously Presented) The wafer of claim 28, wherein the material inhibiting epitaxial growth comprises TEOS.

31. (Previously Presented) The wafer of 28, wherein the material inhibiting epitaxial growth comprises nitride.

32. (Currently Amended) A monolithic wafer of monocrystalline semiconductor material, comprising a plurality of buried trenches and cavity pairs, each trench filled with an epitaxial growth of monocrystalline material, each cavity completely surrounded by said monocrystalline material and having a top formed integral with the wafer and having walls and a closed bottom that are covered with a single coating that is formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned at different heights within the wafer of monocrystalline semiconductor material.

33. (Previously Presented) The wafer of claim 32, wherein the material inhibiting epitaxial growth comprises oxide.

34. (Previously Presented) The wafer of claim 32, wherein the material inhibiting epitaxial growth comprises TEOS.

35. (Previously Presented) The wafer of 32, wherein the material inhibiting epitaxial growth comprises nitride.

36. (New) The structure of claim 8, wherein the coating is in the range of 60 nm to 100 nm.